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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,843	11/25/2002	John Chester Malinowski	BUR920010074	9709

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,843	MALINOWSKI ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-15 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 1-8 and 16-20 in paper mailed on 04/30/2004 is acknowledged.

2. Claims 21-23 are newly added.

3. Claims 9-15 and 21-23 are pending in the application.

Information Disclosure Statement

4. The information disclosure statement filed 01/16/2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because citation number P03 does not corresponds to a proper patent number. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 9, 12, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (U.S. 6,144,051) in view of Allman et al. (6,342,734 B1) and Yaung et al. (U.S. 6,165,880).

In reference to claims 9 and 23, Nishimura et al. (Figs.5A-5E) in a related method to form a MIM capacitor teach forming a metal-insulator-metal (MIM) capacitor including a first metal plate (513), a dielectric layer (514), and a second metal plate (515) formed on the dielectric layer (514); patterning the second metal plate (515); depositing a nitride layer (516) above the MIM capacitor; forming an interlayer dielectric (517) on the nitride layer (516); forming a first via (519) and a second via (521) through the interlayer and the nitride layer (516) by an etching process above the patterned second metal plate and the first metal plate, respectively (column 5, line 51 – column 6, line 15).

Nishimura et al. fail to teach using the nitride layer as an etch stop layer; forming the first and the second via by an anisotropic etch process to contact the nitride layer; and removing portions of the nitride etch stop layer. However, Allman et al. (Figs.1-6) in a related method to form a MIM capacitor teach forming an metal-insulator-metal (MIM) capacitor including a first metal plate (34, 36, 38, 40), a dielectric layer (42) formed on the first metal plate (34, 36, 38, 40), and a second metal plate (44) formed on the dielectric layer (42); patterning the second metal plate (44); depositing a nitride etch stop layer (47) above the MIM capacitor; forming an interlayer dielectric (28) on the nitride etch stop layer (47); forming a first via (56) and a second via (56) through at least the interlayer dielectric (28) by an HDP etch process to contact the nitride etch stop

layer (47); and removing the portions of the nitride etch stop layer (47) (column 4, line 52 – column 8, line 67).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nishimura et al. and Allman et al. to enable the nitride layer of Nishimura et al. to be performed according to the teachings of Allman et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of using the disclosed nitride layer of Nishimura et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Nishimura et al. and Allman fail to teach forming the first and second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer. However, Yaung et al. (Figs.1-3) in a related method to form interconnects using a nitride etch stop layer teach forming a first (1) and a second (1') via through an interlayer dielectric (22) by an anisotropic etch process to contact a nitride etch stop layer (20) (column 5, line 16 – 53). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nishimura et al. and Allman et al. with the teachings of Yaung et al. to enable the etching step of Nishimura et al. and Allman et al. to be performed according to the teachings of Yaung et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching step of Nishimura et al. and Allman et al. and art

recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 12, the combined teachings of Nishimura et al., Allman et al. and Yaung et al. teach depositing the nitride etch stop layer directly upon the MIM capacitor (Nishimura et al., Fig.5B).

In reference to claim 21, the combined teachings of Nishimura et al., Allman et al. and Yaung et al. teach wherein the depositing includes depositing the nitride etch stop layer on at least the first metal plate and the patterned second metal plate (Nishimura et al., Fig.5B).

7. Claims 10, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. ('051) in view of Allman et al. ('734 B1) and Yaung et al. ('880) as applied to claims 9, 12, 21 and 23 above, and further in view of Kai et al. (U.S. 2003/0008467 A1).

In reference to claim 10, the combined teachings of Nishimura et al., Allman et al. and Yaung et al. substantially teach all aspects of the invention but fail to disclose wherein patterning of the second metal plate is accomplished by an anisotropic etch process. However, Kai et al. (Figs.5-11) in a related method to form a MIM capacitor teach patterning a second metal plate (36) using an anisotropic etching process ([0045] – [0050]). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nishimura et al., Allman et al. and Yaung et al. with the teachings of Kai et al. to enable the etching step of Nishimura et al., Allman et al. and Yaung et al. to be performed according to the teachings of Kai et al. because one of

ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching step of Nishimura et al., Allman et al. and Yaung et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 13, the combined teachings of Nishimura et al., Allman et al., Yaung et al. and Kai et al. teach at least etching the dielectric layer by an anisotropic etch process (Kai et al., [0045] – [0050]).

In reference to claim 14, the combined teachings of Nishimura et al., Allman et al., Yaung et al. and Kai et al. teach patterning a wiring level in electrical contact with at least one of the first metal plate and the second metal plate by an anisotropic etch process (column 4, line 52 – column 8, line 67, Yaung et al., column 5, line 16 – 53)

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. ('051) in view of Allman et al. ('734 B1) and Yaung et al. ('880) as applied to claims 9, 12, 21 and 23 above, and further in view of Tsui (U.S. 5,891,799).

The combined teachings of Nishimura et al., Allman et al. and Yaung et al. teach removing portions of the nitride etch stop layer using C_4H_8 (Yaung et al., column 5, lines 37 – 53), but fail to teach removing said portions of the nitride etch stop layer using C_4H_8 and Ar. However, Tsui (Fig.6) in a related method to form interconnects teaches removing portions of a nitride layer (16) using C_4H_8 (column 5, lines 20 – 65). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nishimura et al., Allman et al. and Yaung et al. with the teachings of Tsui to enable the etching step of Nishimura et al., Allman et al. and Yaung et al. to be performed

according to the teachings of Tsui because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed etching step of Nishimura et al., Allman et al. and Yaung et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. ('051) in view of Allman et al. ('734 B1) and Yaung et al. ('880) as applied to claims 9, 12, 21 and 23 above, and further in view of Hsue et al. (U.S. 6,391,713 B1).

The combined teachings of Nishimura et al., Allman et al. and Yaung et al. substantially teach all aspects of the invention but fail to teach forming a second interlayer dielectric between the second metal plate and the nitride etch stop layer. However, Hsue et al. (Figs.3A-3C) in a reduced masking step method of forming a MIM capacitor teach forming a low electrode (126a), a dielectric layer (128a), and a top electrode (130a) of a MIM capacitor; forming a first interlayer dielectric (138) over the top electrode (130a) of the MIM capacitor; forming a nitride etch stop layer (Fig. 3B, 156) over the first interlayer dielectric (138); and forming a second interlayer dielectric (158) over the nitride etch stop layer (156) (column 5, lines 28 – 63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second interlayer dielectric between the nitride etch stop and the top electrode in the combined teachings of Nishimura et al., Allman et al. and Yaung et al. as taught

by Hsue et al., since this would reduce the number of patterning steps during the fabrication of the MIM capacitor (column 1, lines 21 – 52).

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. ('051) in view of Allman et al. ('734 B1) and Yaung et al. ('880) as applied to claims 9, 12, 21 and 23 above, and further in view of Jost et al. (U.S. 6,596,641 B2).

The combined teachings of Nishimura et al., Allman et al. and Yaung et al. substantially teach all aspects of the invention including using dry etching processes to remove portions of the nitride etch stop layer (Yaung et al., column 5, lines 37 – 53), but fail to teach wherein removing portions of the nitride etch stop layer comprises removing the portions buy a wet etch chemistry. However, Jost et al. (Figs.1-6) in a method to form a contact hole (30) teach forming a silicon nitride layer (20) on a surface of a substrate (12) (column 4, lines 1 – 4); forming a silicon oxide layer (25) on the silicon nitride layer (20) (column 6, lines 1 – 24, lines 59 – 67 and column 7, lines 4 – 7); etching the silicon oxide layer (25) using a dry etching process (column 7, lines 54 – 59); and etching the silicon nitride layer (20) using either a dry or wet etching process, thus forming said contact hole (30) (column 7, lines 60 – 63). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Nishimura et al., Allman et al. and Yaung et al. with Jost to enable the etching step of Nishimura et al., Allman et al. and Yaung et al. to be performed according to the teachings of Jost et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed

etching step of Nishimura et al., Allman et al. and Yaung et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

11. Applicant's arguments filed 04/30/2004 have been fully considered but they are not persuasive.

In reference to the Nishimura et al. reference, Applicants argue, "...the Examiner admits that Nishimura fails "to teach using the nitride layer as an etch stop layer; forming the first and second vias by an anisotropic etch process to contact the nitride layer: and removing portions of the nitride etch stop layer...". Furthermore, in reference to the Allman et al. reference, applicants argue. "...Allman clearly show that the optional dielectric laver 47, which allegedly corresponds to the claimed invention's nitride etch stop layer, provides an etch stop for the via extending to the top plate of the capacitor, does not extend over the bottom plate 33 which allegedly corresponds to the claimed invention's first metal plate of the capacitor 20 and thus does not provide an etch stop for the via extending to the top of the bottom plate 33. Therefore, Allman fails to teach or suggest at least the features of "forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer above the patterned second metal plate and above the first metal plate, respectively; and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer," as recited in claim 9..."

In response to applicants arguments, Nishimura et al. teach in Figs.5A-5E a silicon nitride layer 516 deposited over a MIM capacitor, but fail to disclose using said silicon nitride as an etch stop layer. However, Allman et al. et al. teach in Figs.1-6 and related text using silicon nitride layer 47 formed on the upper metal plate and silicon nitride layer 42 formed on the first metal plate as etch stop layers in order to protect the underlying layers, i.e., the first and second metal plates (column 8, lines 21 – 67). Therefore, by using the silicon nitride layer formed in Nishimura et al. as etch stop layer as taught by Allman et al., the MIM capacitor plates 512 and 515 of Nishimura et al. would be protected during the formation of the contact holes 519 and 521.

In response to applicants' arguments, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
July 9, 2004

George Fourson
Primary Examiner